Amendments to the Claims:

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A method for managing data integrity in an adapter, comprising:

receiving data in a receive and/or transmit path;

determining if a cyclic redundancy code ("CRC") mode is enabled; and

selecting a CRC mode from among plural modes including append mode, validate and keep mode, and validate and remove mode; wherein if the append mode is selected, then CRC is appended after each data block boundary.

2. (Previously Presented)The method of Claim 1, wherein adapter firmware code may be used to select a particular mode based on certain register bits.

3. (Previously Presented)The method of Claim 1, wherein if the validate and keep mode is selected, then CRC accompanying any data is compared to accumulated CRC in real time while data is being sent to a host system and if an error occurs after the comparison, an interrupt is generated and data with CRC from a storage system are sent to the host system.

4. (Previously Presented)The method of Claim 1, wherein if the validate and remove mode is selected, then CRC is first validated and then CRC is removed before data is sent, without involving a host system or a storage system and any errors are reported to an adapter processor.

5. (Previously Presented) The method of Claim 1, wherein during an increment mode CRC seed value is incremented for each data block providing a unique CRC value for each data block.

6. (Previously Presented)The method of Claim 5, wherein an optional field and CRC are sent with a data block and the optional field is used to insert custom information.

7. (Previously Presented) A system for managing data integrity in receive and transmit path of an adapter, comprising:

a processor executing firmware code for selecting one of plural ~~CRC~~ modes for implementing cyclic redundancy code ("CRC") including append mode, validate and keep mode, and validate and remove mode, wherein during append mode, a CRC engine determines CRC for each data block and CRC seed value is incremented for each data block such that each data block has a unique CRC value.

8. (Previously Presented) The system of Claim 7, wherein register bits are used for enabling and disabling the plural modes for implementing CRC.

9. (Previously Presented) The system of Claim 7, wherein during the append mode each data block is associated with an optional field for inserting custom information.

10. (Previously Presented) The system of Claim 7, wherein during the validate and keep mode, a CRC engine compares CRC for data with accumulated CRC information in real time while data is being sent to a host system .

11. (Previously Presented) The system of Claim 10,wherein an interrupt is generated if an error occurs after the comparison and CRC received from a storage system in a receive path is sent to the host system.

12. (Previously Presented) The system of Claim 7, wherein during the validate and remove mode, CRC is validated and then CRC information is removed before data is sent without involving a host system or a storage system.

13. (Cancelled)

14. (Currently Amended) An adapter in a redundant array of independent disks ("RAID") controller that is coupled to a host system and a storage media, comprising:

a processor executing firmware code for selecting one of plural modes for implementing cyclic redundancy code ("CRC"),wherein the plural CRC modes include append mode, validate and keep mode, and validate and remove mode and during the append mode, a CRC engine determines CRC for each data block and CRC seed value is incremented for each data block such that each data block has a unique CRC value.

15. (Previously Presented) The adapter of Claim 14, wherein register bits are used for enabling and disabling the plural modes for implementing CRC.

16. (Previously Presented) The adapter of Claim 14, wherein during the append mode each data block is associated with an optional field which is used for inserting custom information.

17. (Previously Presented) The adapter of Claim 14, wherein during the validate and keep mode, a CRC engine compares CRC for-data with accumulated CRC information in real time while data is being sent to the host system.

18. (Previously Presented) The adapter of Claim 17,wherein an interrupt is generated if an error occurs after the comparison and CRC received from the storage system is sent to the host system.

19. (Previously Presented) The adapter of Claim 14, wherein during the validate and remove mode, CRC is validated and CRC information is removed before data is sent without involving the host system or the storage system.

20. (Previously Presented) The adapter of Claim 14, wherein the adapter is coupled to the host system via a PCI and/or PCI-X interface.